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PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicants	:	Vito Fabbrizio et al.
Application No.	:	10/631,323
Filed	:	July 31, 2003
For	:	LOW-VOLTAGE, VERY-LOW-POWER CONDUCTANCE MODE NEURON
Art Unit	:	2122
Docket No.	:	03-I-712 (850063.603RI)
Date	:	May 19, 2005

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Commissioner for Patents
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Alexandria, VA 22313-1450

INFORMATION DISCLOSURE STATEMENT

Commissioner for Patents:

In accordance with 37 CFR 1.56 and 1.97 through 1.98, applicants wish to make known to the U.S. Patent and Trademark Office the references set forth on the attached Form PTO-1449. Copies of the cited U.S. patents and published patent applications are not required and accordingly have not been provided. Copies of all other cited references are enclosed. As to any reference supplied, applicants do not admit that it is "prior art" under 35 U.S.C. §§ 102 or 103, and specifically reserve the right to traverse or antedate any such reference, as by a showing under 37 C.F.R. § 1.131 or other method. Although the aforesaid references are made known to the Patent and Trademark Office in compliance with applicants' duty to disclose all information they are aware of which is believed relevant to the examination of the above-identified application, applicants believe that their invention is patentable.

Please acknowledge receipt of this Information Disclosure Statement and kindly make the cited references of record in the above-identified application.

Applicants believe this Information Disclosure Statement has been timely filed, however, the Commissioner is authorized to charge any fee due by way of this Information Disclosure Statement to our Deposit Account No. 19-1090.

Respectfully submitted,

Seed Intellectual Property Law Group PLLC

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Enclosures:
Form PTO-1449
Cited References (29)

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FORM PTO-1449 (REV. 7-80)	U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE	ATTY. DOCKET NO.	APPLICATION NO.
		03-I-712 (850063.603RI)	10/631,323
	INFORMATION DISCLOSURE STATEMENT (Use several sheets if necessary)	APPLICANTS: Vito Fabbrizio et al.	
		FILING DATE: July 31, 2003	GROUP ART UNIT: 2122

U.S. PATENT DOCUMENTS

*EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE IF APPROPRIATE
	AA	4,956,564	09/11/90	Holler et al.	307	201	
	AB	4,961,002	10/02/90	Tam et al.	307	201	
	AC	4,988,891	01/29/91	Mashiko	307	201	
	AD	5,004,932	04/02/91	Nejime	307	201	
	AE	5,021,693	06/04/91	Shima	307	494	
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	AJ	5,146,602	09/08/92	Holler et al.	395	23	
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	AN		Benson, R. et al., "UV-Activated Conductances Allow for Multiple Time Scale Learning," *IEEE Trans. on Neural Networks 4*(3):434-440, May 1993.
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ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /JH/ (03/04/2009)

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	BC	5,202,956	04/13/93	Mashiko	395	24	
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	BE	5,256,911	10/26/93	Holler et al.	307	201	
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	CD	5,444,821	08/22/95	Li et al.	395	24	
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	CK		Guardiani, C. et al., "Applying a Submicron Mismatch Model to Practical IC Design," in *Proc. of the CICC*, pp. 13.3.1-13.3.1, 1994.
	CL		Holler, M. et al., "An Electrically Trainable Artificial Neural Network (ETANN)with 10240 'Floating Gate' Synapses," in *Proc. IJCNN*, pp. 2.191-2.196, June 1989.
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	DC		Kramer, A. et al., "EEPROM Device as a Reconfigurable Analog Element For Neural Networks," *IEDM Tech. Digest*, pp. 10.3.1-10.3.4, December 1989.
	DD		Kramer, A. et al., "Ultra-Low-Power Analog Associative Memory Core Using Flash-EEPROM-Based Programmable Capacitors," in *Proc. of the 1995 Intl. Symposium on Low Power Design*, Assoc. for Computing Machinery, Dana Point, CA, 1995, pp. 203-208.
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	DK		Seevinck, E. et al., "A Versatile CMOS Linear Transconductor/Square-Law Function Circuit," *IEEE J. Solid-State Circuits SC-22*(3):366-377, June 1987.
	DL		Sin, C-K. et al., "EEPROM as an Analog Storage Device, with Particular Applications in Neural Networks," *IEEE Trans. on Electron Devices 39*(6):1410-1419, June 1992.

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	EE						
	EF						
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	EH					
	EI					
	EJ					

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	EK		Sze, S., *Physics of Semiconductor Devices*, 2 ed., Wiley, 1981, p. 403.
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